Ordering number: EN 3802A

CMOS LSI

No.3802A

LC7233

Single-chip PLL and Microcontroller with LCD Driver

OVERVIEW

The LC7233 is a single-chip microcontroller that incorporates a phase-locked loop (PLL), which can operate up to 150 MHz, and a liquid-crystal display (LCD) driver, making it ideal for digital tuners. It has a large number of input/output ports and a frequency measurement circuit.

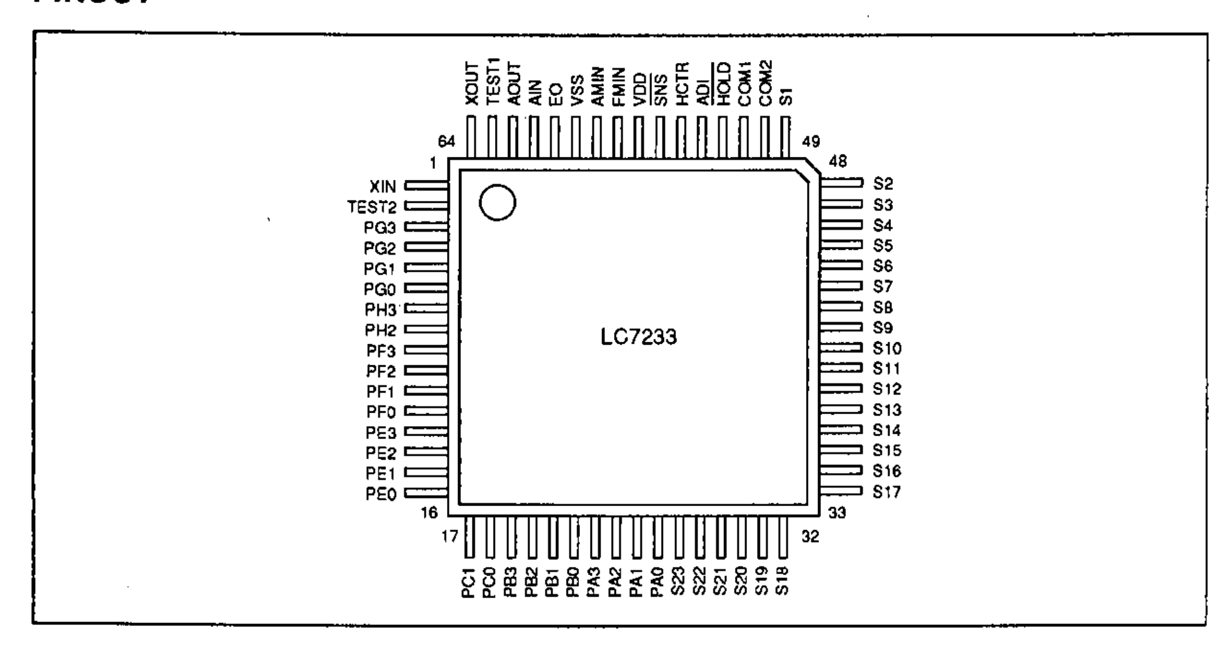
The LC7233 features on-chip RAM and ROM, a programmable high-speed divider, a 6-bit analog-to-digital converter and a low-voltage detection reset circuit.

The LC7233 operates from a single 5 V supply and is available in 64-pin QIPs.

FEATURES

- 150 MHz phase-locked loop
- LCD driver
- 6-bit analog-to-digital converter
- Two 8-bit PWM digital-to-analog converters
- Two 4-bit input ports
- Two 4-bit input/output ports
- 6-bit keypad matrix scan output
- 2-bit open-drain high-voltage output
- 23 mask-selectable output drivers
- 20-bit universal counter
- 4096 × 16-bit program ROM (000H to FFEH user-addressable memory)
- 256 × 4-bit data RAM
- Low-voltage detection reset circuit
- Programmable high-speed divider
- Single-word instructions
- Four-level stack
- PLL-unlocked flip-flop
- Timer flip-flop
- Programmable watchdog interrupt address
- Standby mode
- CPU operates down to 3.5 V, with data retention down to 1.3 V.
- Single 5 V supply
- 64-pin QIP

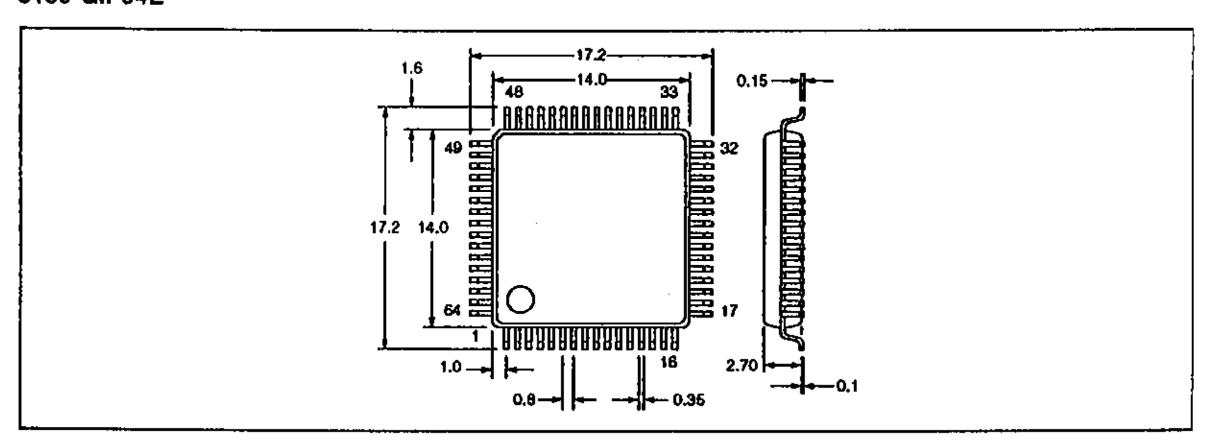
PINOUT



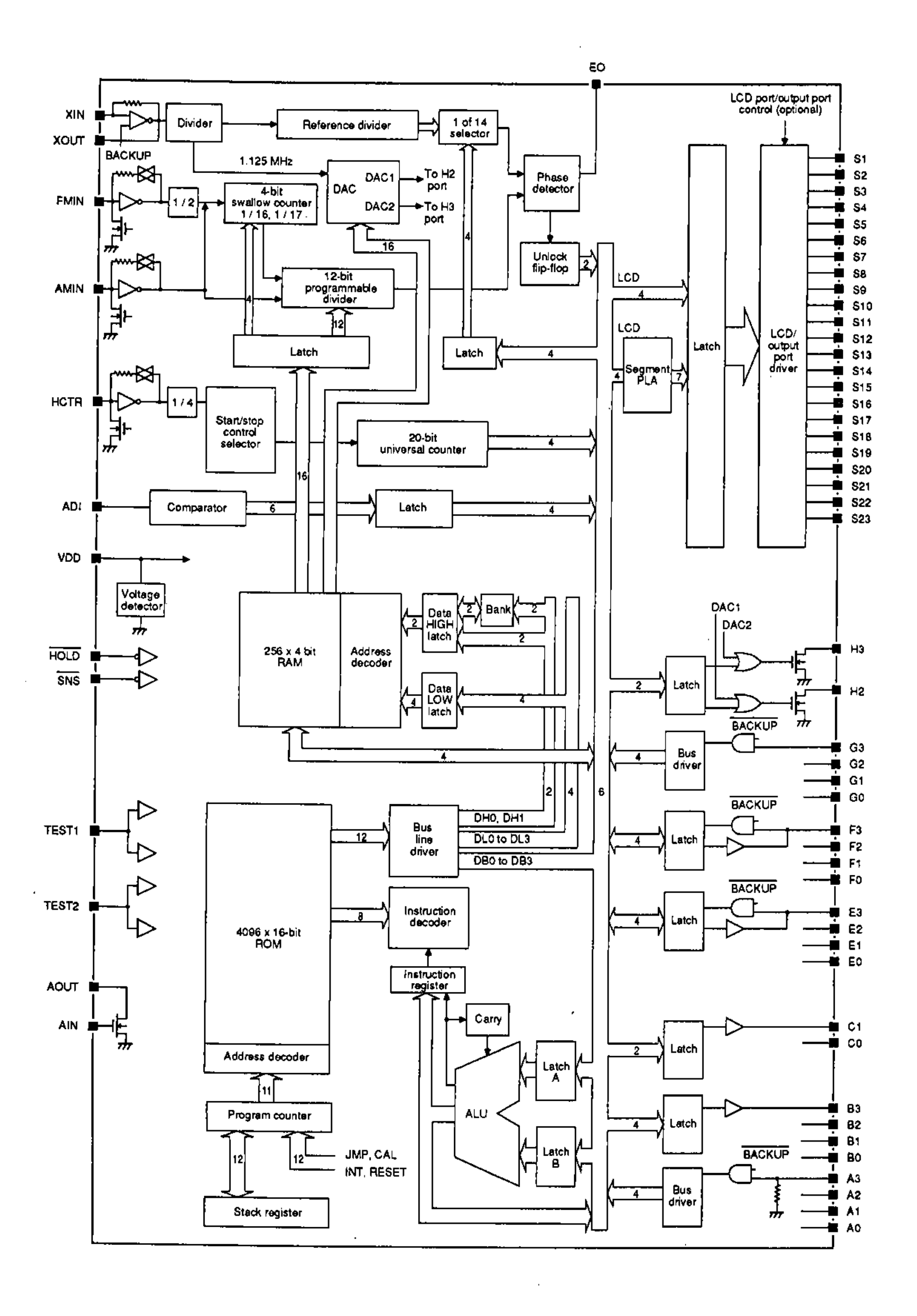
PACKAGE DIMENSIONS

Unit: mm

3159-QIP64E



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Equivalent circuit	Description
1	XIN	XIN, XOUT	Crystal oscillator connections
64	XOUT		
2	TEST2		Test pins
63	TEST1		
3 to 6	PG3 to PG0	BACKUP	Input port G
7, 8	PH1, PH0	BACKUP	Output port H
9 to 12	PF3 to PF0	BACKUP	Input/output port F
13 to 16	PE3 to PE0		Input/output port E
17, 18	PC1, PC0	BACKUP	Output port C
19 to 22	PB3 to PB0		Output port B
23 to 26	PA3 to PA0	BACKUP, Mask option	Input port A

Number	Name	Equivalent circuit	Description
27 to 49	S23 to S1	BACKUP	LCD segment outputs
50, 51	COM2, COM1	$\overline{\text{BACKUP}}$	LCD common driver outputs
52	$\overline{\text{HOLD}}$		Hold-mode control input
55	$\overline{\text{SNS}}$		Power-fail detect
53	ADI	ref HOLD, PLLSTOP controlled	A/D converter input
54	HCTR	HOLD, PLLSTOP controlled	Universal counter input
56	VDD		5 V supply
57	FMIN	HOLD, PLLSTOP controlled	FM VCO input
58	AMIN		AM VCO input
59	VSS		Ground

Number	Name	Equivalent circuit	Description
60	EO		Phase comparator output
61	AIN		Analog input
62	AOUT		Analog output

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD} max	–0.3 to 6.5	V
Port G, $\overline{HOLD}$, ADI and $\overline{SNS}$ input voltage range	V_{IN1}	–0.3 to 13	V
Input voltage range (other inputs)	V_{IN2}	–0.3 to V_{DD} + 0.3	V
Port H and AOUT output voltage range	V_{OUT1}	–0.3 to 15	V
Output voltage range (all other outputs)	V_{OUT2}	–0.3 to V_{DD} + 0.3	V
Port H output current range	I_{OUT1}	0 to 5	mA
Ports E and F output current range	I_{OUT2}	0 to 3	mA
Ports B and C output current range	I_{OUT3}	0 to 1	mA
AOUT output current range	I_{OUT4}	0 to 2	mA
Power dissipation	P_D	400	mW
Operating temperature range	Topr	–40 to 85	deg. C
Storage temperature range	T_{stg}	–45 to 125	deg. C

Recommended Operating Conditions

T_a = 25 deg. C

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	5	V
Supply voltage range (PLL and CPU)	V_{DD1}	4.5 to 5.5	V
Supply voltage range (CPU)	V_{DD2}	3.5 to 5.5	V
Supply voltage range for data retention	V_{DD3}	1.3 to 5.5	V

Electrical Characteristics

V_{DD} = 3.5 to 5.5 V, T_a = –40 to 85 deg. C unless otherwise noted

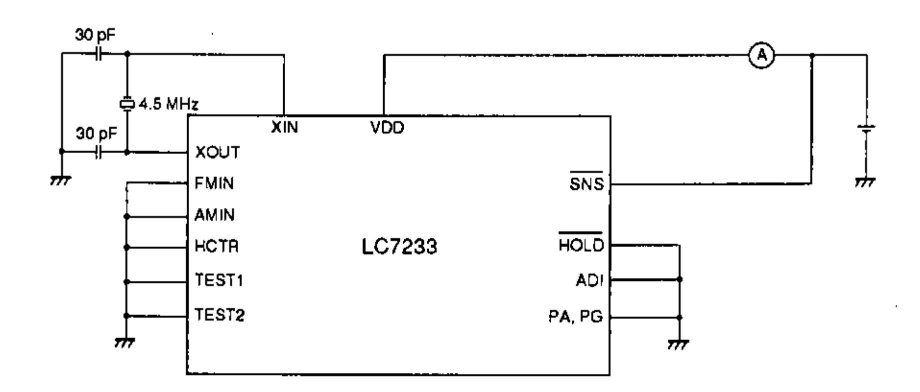
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Port G HIGH-level input voltage	V_{IH1}		0.7V_{DD}	–	8.0	V
$\overline{SNS}$ HIGH-level input voltage	V_{IH2}		2.5	–	8.0	V
Port A HIGH-level input voltage	V_{IH3}		0.6V_{DD}	–	V_{DD}	V
Ports E and F HIGH-level input voltage	V_{IH4}		0.7V_{DD}	–	V_{DD}	V
$\overline{HOLD}$ HIGH-level input voltage	V_{IH5}		0.8V_{DD}	–	8.0	V
Port G LOW-level input voltage	V_{IL1}		0	–	0.3V_{DD}	V
$\overline{HOLD}$ LOW-level input voltage	V_{IL2}		0	–	0.4V_{DD}	V
$\overline{SNS}$ LOW-level input voltage	V_{IL3}		0	–	1.3	V
Port A LOW-level input voltage	V_{IL4}		0	–	0.2V_{DD}	V
Ports E and F LOW-level input voltage	V_{IL5}		0	–	0.3V_{DD}	V
XIN input frequency	f_{IN1}	V_{IN} = 0.5 to 1.5 V	4.0	4.5	5.0	MHz
FMIN input frequency	f_{IN2}	V_{IN} = 0.1 to 1.5 V, V_{DD} = 4.5 to 5.5 V	10	–	130	MHz
		V_{IN} = 0.15 to 1.5 V, V_{DD} = 4.5 to 5.5 V	10	–	150	
AMIN input frequency (low range)	f_{IN3}	V_{IN} = 0.1 to 1.5 V, V_{DD} = 4.5 to 5.5 V	0.5	–	10	MHz
AMIN input frequency (high range)	f_{IN4}	V_{IN} = 0.1 to 1.5 V, V_{DD} = 4.5 to 5.5 V	2.0	–	40	MHz
HCTR input frequency	f_{IN5}	V_{IN} = 0.1 to 1.5 V, V_{DD} = 4.5 to 5.5 V	0.4	–	12	MHz
XIN rms input amplitude	V_{IN1}		0.5	–	1.5	V
FMIN rms input amplitude	V_{IN2}		0.1	–	1.5	V
AMIN rms input amplitude	V_{IN3}		0.1	–	1.5	V
HCTR rms input amplitude	V_{IN4}		0.1	–	1.5	V
ADI input voltage range	V_{IN5}		0	–	V_{DD}	V
$\overline{SNS}$ reject pulsewidth	P_{rej}		–	–	50	µs
Standby threshold voltage	V_{DET}		2.7	3.0	3.3	V
$\overline{HOLD}$, ADI, $\overline{SNS}$ and port G HIGH-level input current	I_{IH1}	V_{IN} = 5.5 V	–	–	3.0	µA
Ports A, E and F HIGH-level input current	I_{IH2}	Ports E and F are high impedance, port A has no R_{PD}, V_{IN} = V_{DD}	–	–	3.0	µA
XIN HIGH-level input current	I_{IH3}	V_{IN} = V_{DD} = 5.0 V	2	5	15	µA
FMIN, AMIN and HCTR HIGH-level input current	I_{IH4}	V_{IN} = V_{DD} = 5.0 V	4	10	30	µA
Port A HIGH-level input current	I_{IH5}	V_{IN} = V_{DD} = 5.0 V, port A has R_{PD}	–	50	–	µA
AIN HIGH-level input current	I_{IH6}	V_{IN} = V_{DD}	–	0.01	10.00	nA

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
$\overline{HOLD}$, ADI, $\overline{SNS}$ and port G LOW-level input current	I_{IL1}	V_{IN} = V_{SS}	–	–	3.0	μA
Ports A, E and F LOW-level input current	I_{IL2}	Ports E and F are high impedance, port A has no R_{PD}, V_{IN} = V_{SS}	–	–	3.0	μA
XIN LOW-level input current	I_{IL3}	V_{IN} = V_{SS}	2	5	15	μA
FMIN, AMIN and HCTR LOW-level input current	I_{IL4}	V_{IN} = V_{SS}	4	10	30	μA
AIN LOW-level input current	I_{IL5}	V_{IN} = V_{SS}	–	0.01	10.0	nA
Port A input voltage	V_{IF}	Port A is high impedance	–	–	0.05V_{DD}	V
Port A pull-down resistance	R_{PD}	V_{DD} = 5 V	75	100	200	kΩ
EO output leakage current	I_{OFFH1}	V_O = V_{DD}	–	0.01	10.0	nA
Ports B, C, E and F output leakage current	I_{OFFH2}	V_O = V_{DD}	–	–	3.0	μA
Port H output leakage current	I_{OFFH3}	V_O = 13 V	–	–	5.0	μA
AOUT output leakage current	I_{OFFH4}	V_O = 13 V	–	–	1.0	μA
EO output leakage current	I_{OFFL1}	V_O = V_{SS}	–	0.01	10.0	nA
Ports B, C, E and F output leakage current	I_{OFFL2}	V_O = V_{SS}	–	–	3.0	μA
Ports B and C HIGH-level output voltage	V_{OH1}	I_O = 1 mA	V_{DD} – 2.0	V_{DD} – 1.0	V_{DD} – 0.5	V
Ports E and F HIGH-level output voltage	V_{OH2}	I_O = 1 mA	V_{DD} – 1.0	–	–	V
EO HIGH-level output voltage	V_{OH3}	I_O = 500 μA	V_{DD} – 1.0	–	–	V
XOUT HIGH-level output voltage	V_{OH4}	I_O = 200 μA	V_{DD} – 1.0	–	–	V
S1 to S23 HIGH-level output voltage	V_{OH5}	I_O = –0.1 mA	V_{DD} – 1.0	–	–	V
COM1 and COM2 HIGH-level output voltage	V_{OH6}	I_O = 25 μA	V_{DD} – 0.75	–	–	V
Ports B and C LOW-level output voltage	V_{OL1}	I_O = 50 μA	0.5	1.0	2.0	V
Ports E and F LOW-level output voltage	V_{OL2}	I_O = 1 mA	–	–	1.0	V
EO LOW-level output voltage	V_{OL3}	I_O = 500 μA	–	–	1.0	V
XOUT LOW-level output voltage	V_{OL4}	I_O = 200 μA	–	–	1.0	V
S1 to S23 LOW-level output voltage	V_{OL5}	I_O = 0.1 mA	–	–	1.0	V
AOUT LOW-level output voltage	V_{OL6}	I_O = 5 mA, AIN = 1.3 V	–	–	0.5	V
COM1 and COM2 LOW-level output voltage	V_{OL7}	I_O = 25 μA	0.3	0.5	0.75	V
Port H LOW-level output voltage	V_{OL8}	I_O = 5 mA	0.75	–	2.0	V
COM1 and COM2 mid-level output voltage	V_{M1}	V_{DD} = 5 V, I_O = 20 μA	2.0	2.5	3.0	V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
A/D converter error	ε	V_{DD} = 4.5 to 5.5 V	– ½	–	½	lsb
Supply current	I_{DD1}	f_{in} = 130 MHz, V_{DD} = 4.5 to 5.5 V	–	15	20	mA
Hold-mode supply current	I_{DD2}	PLL halted, t_{cyc} = 2.67 μs	–	1.5	–	mA
		PLL halted, t_{cyc} = 13.33 μs, V_{DD} = 3.5 to 5.5 V	–	1.0	–	
		PLL halted, t_{cyc} = 40.00 μs, V_{DD} = 3.5 to 5.5 V	–	0.7	–	
Standby-mode supply current	I_{DD3}	V_{DD} = 5.5 V, oscillator halted, T_a = 25 deg. C	–	–	5	μA
		V_{DD} = 2.5 V, oscillator halted, T_a = 25 deg. C	–	–	1	

Measurement Circuits

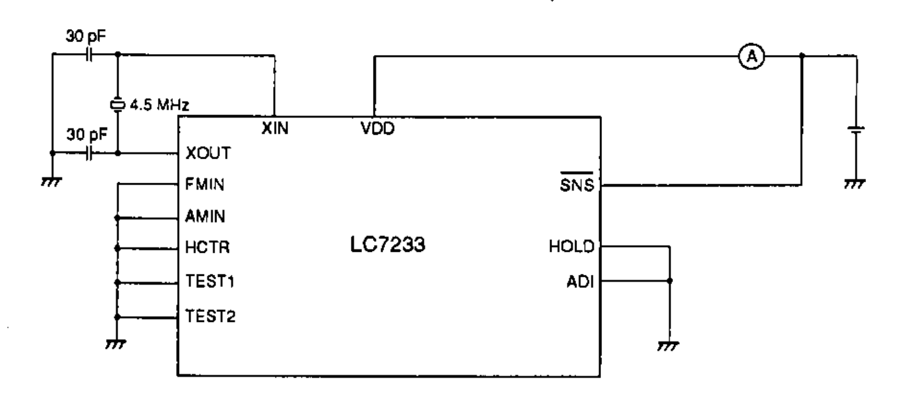
Hold mode



Notes

1. Ports E and F are selected as output ports.
2. Ports A to H, S1 to S23, COM1 and COM2 are open.

Standby mode



Note

Ports A to H, S1 to S23, COM1 and COM2 are open.

FUNCTIONAL DESCRIPTION

LCD Driver

The LC7233 can drive LCD segments. The LCP and LCD instructions transfer data to the LCD outputs. The LCD instruction transfers data directly to the LCD outputs. The LCP instruction converts data to 7-segment format before transfer to the outputs.

S1 to S23 are the driver outputs. The LCD frame rate is 100 Hz with a 50% duty cycle. After reset or power-up, a blank signal is present on all outputs. In standby mode, all outputs are LOW. They can be used as general-purpose outputs if the appropriate mask option is selected.

COM1 and COM2 are the LCD common driver outputs. Output drive is 50% duty with 50% bias. Upon reset or after power-up, the normal drive signals are present on these outputs. In standby mode, all outputs are LOW.

Frequency Counter

Frequency measurement is performed at the HCTR input by the 20-bit universal counter. The input frequency range is 0.4 to 12 MHz, which is used for measuring AM and FM IF frequencies. Capacitive coupling should be used.

Phase-locked Loop

The FMIN or AMIN input signal is divided down by a programmable divider, and then compared with the crystal frequency, which is also divided down using 14 selectable ratios. The phase difference between the two signals is measured using a phase detector and output on EO.

FMIN is the input pin for the FM VCO input signal. The input frequency range is 10 to 130 MHz. Capacitive coupling should be used.

AMIN is the AM VCO input. The bandwidth is adjustable in two ranges by using the PLL instruction—HIGH (2 to 40 MHz) for the SW band, and LOW (0.5 to 10 MHz), for the LW and MW bands. Capacitive coupling should be used.

Input/Output Ports

Port A

This input port has a low switching threshold, which is used for keypad matrix inputs. Pull-down resistors for all pins are available as a mask option. Note that either all or none of the pins should have pull-down resistors. In standby mode, inputs are ignored.

Ports B and C

These output ports have unbalanced CMOS outputs which are used as keypad matrix scan outputs. Upon reset, outputs are set LOW, and in standby mode, outputs are high impedance. The outputs can be short-circuited.

Port E

The transfer direction of this input/output port is selected automatically under software control. When an input instruction (IN, TPT, or TPF) is executed, port E is configured for input operation, and an output instruction (OUT, SPB or RPB), for output operation. Upon reset, all pins become inputs. In standby mode, the output drivers are high impedance and the input signals are ignored. All bits should either be inputs or outputs.

Port F

The transfer direction of this input/output port is selected by the FPC instruction. Each pin of this port can be set independently to be an input or output. Upon reset, all pins become inputs. In standby mode, the output drivers are high impedance and the input signals are ignored.

Port G

This is an input port only. In standby mode, inputs are ignored.

Port H

These output ports are high-voltage, n-channel open-drain drivers, which are used for switching power supplies. Upon reset and in standby mode, outputs are high impedance. Port H can also be configured as the output of DACI and DAC2.

A/D Converter

The A/D converter is a 6-bit successive approximation type. The conversion cycle time is 1.28 ms. Full-scale output data is 3FH for an input of $V_{DD} \times (63/96)$.

Power-fail Detection

When connected to the supply, $\overline{SNS}$ is used as a power-fail detector. $\overline{SNS}$ can also be used as a standard input port.

Crystal Oscillator

The master crystal oscillator, which has a feedback resistor on-chip, requires only the connection of a 4.5 MHz crystal.

Low-power Modes

Hold mode

When the hold-mode control pin, $\overline{HOLD}$, is driven LOW and the HOLDEN (hold enable) flip-flop has previously been set by an SS instruction, the LC7233 enters hold mode.

$\overline{HOLD}$ has a high-voltage input (V_{IH}(max) = 8.0 V) which can be connected directly to the power supply.

Standby mode

When the LC7233 is in hold mode and $\overline{HOLD}$ is LOW, standby mode can be set by the CKSTP instruction.

Test Pins

Two device test pins are provided—TEST1 and TEST2. These should either be tied to V_{SS} or left open.

INSTRUCTION SET

ADDR	Program memory address [12 bits]
b	Borrow
B	Bank number [2 bits]
C	Carry
DH	Data memory address high-order bits (row address) [2 bits]
DL	Data memory address low-order bits (column address) [4 bits]
I	Immediate data [4 bits]
M	Data memory address
N	Bit position [4 bits]
Pn	Port number [4 bits]
r	General register (Bank 00H to 0FH)
Rn	Register number [4 bits]
( )	Contents of register or memory
( )n	Contents of bit N of register or memory

Mnemonic	Operand		Operation	Instruction format																Notation	Description	Skip condition
	1st	2nd		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0			
Add instructions																						
AD	r	M	Add M to r	0	1	0	0	0	0	DH		DL				Rn				r ← (r) + (M)	Adds the contents of M to the contents of r and stores the result in r	
ADS	r	M	Add M to r and skip if carry	0	1	0	0	0	1	DH		DL				Rn				r ← (r) + (M), skip if carry	Adds the contents of M to the contents of r and stores the result in r. Skips if a carry is generated	Carry
AC	r	M	Add M to r with carry	0	1	0	0	1	0	DH		DL				Rn				r ← (r) + (M) + C	Adds the contents of M to the contents of r and C and stores the result in r	
ACS	r	M	Add M to r with carry and skip if carry	0	1	0	0	1	1	DH		DL				Rn				r ← (r) + (M) + C, skip if carry	Adds the content of M to the contents of r and C and stores the result in r. Skips if a carry is generated	Carry
AI	M	I	Add I to M	0	1	0	1	0	0	DH		DL				I				M ← (M) + I	Adds the immediate data to the contents of M and stores the result in M	
AIS	M	I	Add I to M and skip if carry	0	1	0	1	0	1	DH		DL				I				M ← (M) + I, skip if carry	Adds the immediate data to the contents of M and stores the result in M. Skips if a carry is generated	Carry
AIC	M	I	Add I to M with carry	0	1	0	1	1	0	DH		DL				I				M ← (M) + I + C	Adds the immediate data to the contents of M and C and stores the result in M	
AICS	M	I	Add I to M with carry and skip if carry	0	1	0	1	1	1	DH		DL				I				M ← (M) + I + C, skip if carry	Adds the immediate data to the contents of M and C and stores the result in M. Skips if a carry is generated	Carry
Subtract instructions																						
SU	r	M	Subtract M from r	0	1	1	0	0	0	DH		DL				Rn				r ← (r) − (M) skip if carry	Subtracts the contents of M from the contents of r and stores the result in r	
SUS	r	M	Subtract M from r and skip if borrow	0	1	1	0	0	1	DH		DL				Rn				r ← (r) − (M), skip if borrow	Subtracts the contents of M from the contents of r and stores the result in r. Skips if a borrow is generated	Borrow
SB	r	M	Subtract M from r with borrow	0	1	1	0	1	0	DH		DL				Rn				r ← (r) − (M) − b	Subtracts the contents of M from the contents of r with borrow and stores the result in r	
SBS	r	M	Subtract M from r with borrow and skip if borrow	0	1	1	0	1	1	DH		DL				Rn				r ← (r) − (M) − b, skip if borrow	Subtracts the contents of M from the contents of r with borrow and stores the result in r. Skips if a borrow is generated	Borrow
SI	M	I	Subtract I from M	0	1	1	1	0	0	DH		DL				I				M ← (M) − I	Subtracts the immediate data from the contents of M and stores the result in M	
SIS	M	I	Subtract I from M and skip if borrow	0	1	1	1	0	1	DH		DL				I				M ← (M) − I, skip if borrow	Subtracts the immediate data from the contents of M and stores the result in M. Skips if a borrow is generated	Borrow
SIB	M	I	Subtract I from M with borrow	0	1	1	1	1	0	DH		DL				I				M ← (M) − I − b	Subtracts the immediate data from the contents of M with borrow and stores the result in M	

Mnemonic	Operand		Operation	Instruction format																Notation	Description	Skip condition
	1st	2nd		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0			
SIBS	M	I	Subtract I from M with borrow and skip if borrow	0	1	1	1	1	1	DH		DL				I				M ← (M) − I − b, skip if borrow	Subtracts the immediate data from the contents of M with borrow and stores the result in M. Skips if a borrow is generated	Borrow
Compare instructions																						
SEQ	r	M	Skip if r equals M	0	0	0	0	0	1	DH		DL				Rn				(r) − (M), skip if zero	Compares the contents of r and M and skips if they are equal	(r) = (M)
SGE	r	M	Skip if r is greater than or equal to M	0	0	0	0	1	1	DH		DL				Rn				(r) − (M), skip if (r) ≥ (M)	Compares the contents of r and M and skips if r is greater than or equal to M	(r) ≥ (M)
SEQI	M	I	Skip if M equals I	0	0	1	1	0	1	DH		DL				I				(M) − I, skip if zero	Compares the immediate data to the contents of M and skips if they are equal	(M) − I = 0
SGEI	M	I	Skip if M is greater than or equal to I	0	0	1	1	1	1	DH		DL				I				(M) − I, skip if (M) ≥ I	Compares the contents of M with the immediate data and skips if M is greater than or equal to I	(M) ≥ I
Logic arithmetic instructions																						
AND	M	I	AND I with M	0	0	1	1	0	0	DH		DL				I				M ← (M) · I	Calculates the logic-AND of the immediate data and the contents of M and stores the result in M	
OR	M	I	OR I with M	0	0	1	1	1	0	DH		DL				I				M ← (M) + I	Calculates the logic-OR of the immediate data and the contents of M and stores the result in M	
EXL	r	M	Exclusive-OR M with r	0	0	1	0	0	0	DH		DL				Rn				r ← (r) oplus (M)	Calculates the logic-XOR of the contents of r and M, and stores the result in r	
Load and store instructions																						
LD	r	M	Load M into r	1	0	0	0	0	0	DH		DL				Rn				r ← (M)	Moves the contents of M to r	
ST	M	r	Store r in M	1	0	0	0	0	1	DH		DL				Rn				M ← (r)	Moves the contents of r to M	
MVRD	r	M	Move M to M addressed by Rn	1	0	0	0	1	0	DH		DL				Rn				[DH, Rn] ← (M)	Moves the contents of M to the address referenced by DH and Rn	
MVRS	M	r	Move M addressed by Rn to M	1	0	0	0	1	1	DH		DL				Rn				M ← [DH, Rn]	Moves the contents of the memory location referenced by DH and Rn to M	
MVSR	M_1	M_2	Move M to M	1	0	0	1	0	0	DH		DL_1				DL_2				[DH.DL_1] ← [DH.DL_2]	Moves the contents of memory location 2 to memory location 1	
MVI	M	I	Move I to M	1	0	0	1	0	1	DH		DL				I				M ← I	Moves the immediate data to M	
PLL	M	r	Load M to PLL registers	1	0	0	1	1	0	DH		DL				Rn				PLLr ← (M)	Moves the contents of M to the PLL registers	

Mnemonic	Operand 1st	Operand 2nd	Operation	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Notation	Description	Skip condition
Bit test instructions																						
TMT	M	N	Test bits of M and skip if true	1	0	1	0	0	1	DH		DL				N				Skip if M(N) = all 1	Tests the bits of memory location M specified by N. Skips if all bits are logic 1	All bits specified = 1
TMF	M	N	Test bits of M and skip if false	1	0	1	0	1	1	DH		DL				N				Skip if M(N) = all 0	Tests the bits of memory location M specified by N. Skips if all bits are logic 0	All bits specified = 0
Jump and subroutine instructions																						
JMP	ADDR		Jump to address	1	0	1	1	ADDR (12 bits)												PC ← ADDR	Jumps to the address specified by ADDR	
CAL	ADDR		Call subroutine	1	1	0	0	ADDR (12 bits)												Stack ← (PC) + 1, PC ← ADDR	Jumps to the subroutine specified by ADDR	
RT			Return from subroutine	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	PC ← stack	Returns from a subroutine	
Flag test instructions																						
TTM	N		Test timer flip-flop	1	1	0	1	0	1	1	0	0	0	0	0	N				Skip if timer F/F = 0	Tests the timer flip-flop and skips if zero	Timer F/F = 0
TUL	N		Test PLL flip-flop	1	1	0	1	0	1	1	1	0	0	0	0	N				Skip if PLL F/F = 0	Tests the PLL-unlocked flip-flop and skips if zero	PLL F/F = 0
Status register test and set instructions																						
SS	N		Set status register bits	1	1	0	1	1	1	0	0	0	0	0	0	N				(Status register 1) N ← 1	Sets the bits of the status register specified by N	
RS	N		Reset status register bits	1	1	0	1	1	1	0	1	0	0	0	0	N				(Status register 1) N ← 0	Resets the bits of the status register specified by N	
TST	N		Test status register bits and skip if true	1	1	0	1	1	1	1	0	0	0	0	0	N				Skip if (status register 2) N = all 1	Tests the bits of status register 2 specified by N. Skips if all bits are 1	All bits specified = 1
TSF	N		Test status register bits and skip if false	1	1	0	1	1	1	1	1	0	0	0	0	N				Skip if (status register 2) N = all 0	Tests the bits of status register 2 specified by N. Skips if all bits are 0	All bits specified = 0
Bank select instruction																						
BANK	B		Select bank	1	1	0	1	0	0	B		0	0	0	0	0	0	0	0	BANK ← B	Selects one of four memory banks	
Input/output instructions																						
LCD	M	I	Move data to LCD segments	1	1	1	0	0	0	DH		DL				DIGIT				LCD (DIGIT) ← I	Loads the immediate data directly to the LCD driver	
LCP	M	I	Move 7-segment data to LCD	1	1	1	0	0	1	DH		DL				DIGIT				LCD (DIGIT) ← PLA ← I	Converts the immediate data to 7-segment format using a PLA then transfers it to the LCD driver	
IN	M	Pn	Move port data to M	1	1	1	0	1	0	DH		DL				P				M ← (port (Pn))	Moves the data from input port Pn to M	

Mnemonic	Operand		Operation	Instruction format																Notation	Description	Skip condition
	1st	2nd		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0			
OUT	M	Pn	Move data to port	1	1	1	0	1	1	DH		DL				P				(Port (Pn)) ← M	Moves the contents of memory location M to port Pn	
SPB	Pn	N	Set port bits	1	1	1	1	0	0	0	0	P				N				(Port (Pn)) N ← 1	Sets the bits of port Pn, specified by N, to logic 1	
RPB	Pn	N	Reset port bits	1	1	1	1	0	1	0	1	P				N				(Port (Pn)) N ← 0	Sets the bits of port Pn, specified by N, to logic 0	
TPT	Pn	N	Test bits of port and skip if true	1	1	1	1	1	0	1	0	P				N				Skip if (port (Pn)) N = all 1	Tests the bits of port Pn specified by N. Skips if all bits are logic 1	All bits specified = 1
TPF	Pn	N	Test bits of port and skip if false	1	1	1	1	1	1	1	1	P				N				Skip if (port (Pn) N = all 0	Tests the bits of port Pn specified by N. Skips if all bits are logic 0	All bits specified = 0
Universal counter instructions																						
UCS	I		Set UCCW1	0	0	0	0	0	0	0	1	0	0	0	0	I				UCCW1 ← 1	Sets the universal counter flag 1	
UCC	I		Set UCCW2	0	0	0	0	0	0	1	1	0	0	0	0	I				UCCW2 ← 1	Sets the universal counter flag 2	
Miscellaneous instructions																						
FPC	N		Port F direction control	0	0	0	1	0	0	0	0	0	0	0	0	N				FPC latch ← N	Defines the direction of individual pins of port F. If a bit in the port F direction register is set by FPC, the corresponding pin of port F becomes an output.	
CKSTP			Stop clock	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	Stop clock if $\overline{HOLD}$ = 0	Stops the processor clock if $\overline{HOLD}$ = 0	
DAC	I		Move data to DAC registers	0	0	0	0	0	0	1	0	0	0	0	0	I				DAC_r ← I	Loads the immediate data to the DAC registers	
NOP			No operation	0	0	0	0	0	0	0	0	0	0	0	0						No operation	

MASK OPTIONS

Parameter	Options
Watchdog timer (WDT)	Yes
	No
Pull-down resistors on port A (the keypad matrix input port)	Yes
	No
Instruction cycle time	2.67 μs
	13.33 μs
	40.00 μs
S1 to S23 configuration	LCD driver output port
	General-purpose output port

DEVELOPMENT SYSTEM

The LC7233 development environment is shown in figure 1. It uses an LC72EV32 evaluation chip mounted on a TB-72EV32 target board and a multifunctional emulator (RE32), which is controlled by a personal computer, to provide full debugging facilities.

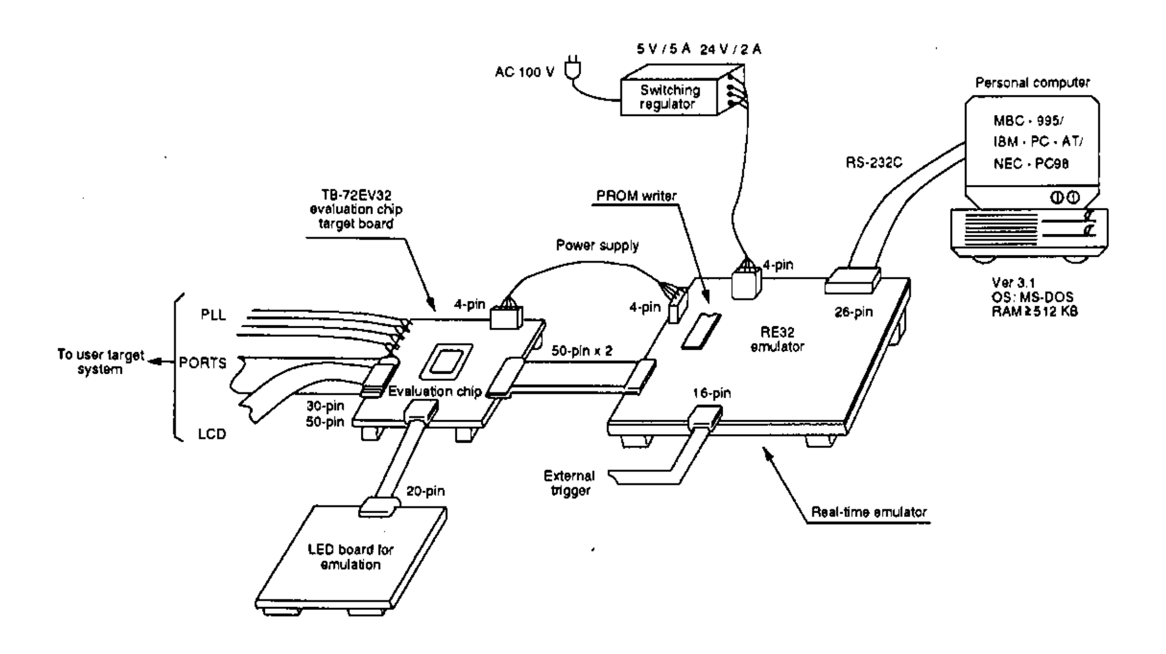


Figure 1. Development system